dielectric isolation structure is formed to a depth, within a substrate upon which the ESD device is formed, that is relatively shallower than other dielectric isolation structures, such as shallow trench isolation (STI) or deep trench isolation. In this way, current flows substantially under the dielectric isolation structure along a relatively shorter path having a lower resistance than a longer path that would otherwise be traveled if the dielectric isolation structure was formed deeper within the substrate. Because the current flows along the shorter path with the lower resistance, the ESD device can handle a larger current before failure, such as failure resulting from a thermal event caused by high power dissipation.

[0014] According to some embodiments of the present disclosure, an ESD device comprises a first doped region formed within a substrate upon which the ESD device is formed. For example, the first doped region comprises a collector that is doped according to a first doping polarity. The ESD device comprises a second doped region formed within the substrate. For example, the second doped region comprises an emitter that is doped according to the first doping polarity. The first doped region and the second doped region are formed such that current flows from the second doped region to the first doped region during an ESD event. In an embodiment, the first doped region corresponds to an emitter of the ESD device. In an embodiment, the second doped region corresponds to a collector of the ESD device. A dielectric isolation structure is formed between the first doped region and the second doped region at a depth that is less than at least one of a first depth of the first doped region or a second depth of the second doped region. In an embodiment, the dielectric isolation structure is formed between the first doped region and the second doped region such that a bottom surface of the dielectric isolation structure is formed to a depth that is less than at least one of a depth of a bottom surface of the first doped region or a depth of a bottom surface of the second doped region. In an embodiment, a bottom surface of the dielectric isolation structure is formed to be substantially flush with a surface of the substrate, such as a silicon surface, for example. In an embodiment, the ESD device comprises a third doped region within the substrate. For example, the third doped region comprises a base for the ESD device. The third doped region is doped according to a second doping polarity that is different than the first doping polarity.

[0015] In an embodiment, the dielectric isolation structure comprises a resist protective oxide (RPO) layer. In an embodiment, the dielectric isolation structure does not comprise shallow trench isolation (STI). It may be appreciated that various types of isolation structures can be used for the dielectric isolation structure. In this way, current, flowing from the one of the doped regions to another doped region during an ESD event, flows substantially under the dielectric isolation structure. Because the dielectric isolation structure is formed at a relatively shallower depth, such as compared to the first doped region or the second doped region, current flows along a relatively short path from one of the doped regions to another doped region.

[0016] In an embodiment of the ESD device, the ESD device comprises a bipolar junction transistor (BJT). The first doped region of the BJT comprises a collector connected to lower voltage level, such as VSS, during normal operation. The second doped region of the BJT comprises an emitter connected to higher voltage level, such as VDD, during normal operation. During an ESD event, current flows from one of the terminals, substantially under the dielectric isolation structure, to another terminal. In an embodiment of the ESD device, the ESD device comprises a diode. The first doped region of the diode comprises an anode connected to lower voltage level, such as VSS, during normal operation. The second doped region of the diode comprises a cathode connected to higher voltage level, such as VDD, during normal operation. During an ESD event, current flows from one of the terminals, substantially under the dielectric isolation structure, to another terminal. In an embodiment of the ESD device, the ESD device comprises a silicon control rectifier. The first doped region of the silicon control rectifier comprises a cathode connected to lower voltage level, such as VSS, during normal operation. The second doped region of the silicon control rectifier comprises an anode connected to higher voltage level, such as VDD, during normal operation. During an ESD event, current flows from one of the terminals, substantially under the dielectric isolation structure, to another terminal. It may be appreciated that some embodiments of the ESD device are illustrated in FIGS. **2**A and **2**B.

[0017] According to some embodiments of the present disclosure, an apparatus comprises an ESD device. The ESD device comprises a collector formed within a substrate upon which the ESD device is formed. The collector comprises a first doped region that is doped according to a first doping polarity. The ESD device comprises an emitter formed within the substrate. The emitter comprises a second doped region that is doped according to the first doping polarity. The ESD device comprises a dielectric isolation region formed between the collector and the emitter. The dielectric isolation structure comprises a resist protective oxide (RPO) layer. The RPO layer is configured to provide isolation between the collector and the emitter. In an embodiment, the RPO layer is formed to a depth that is less than at least one of a first depth of the first doped region of the collector or a second depth of the second doped region of the emitter. In an embodiment, the RPO layer is formed on top of a surface of the substrate. In an embodiment, the RPO layer comprises a silicide blocking layer.

[0018] In an embodiment, the apparatus comprises an integrated circuit. The ESD device is operably coupled to the integrated circuit, such that the ESD device protects the integrated circuit from relatively high current during an ESD event that would otherwise damage the integrated circuit. In particular, the ESD device is configured to become active during the ESD event. While active, current flows from one of the terminals, substantially under the dielectric isolation region, to another terminal in order to divert the current away from the integrated circuit. It may be appreciated that some embodiments of the ESD device are illustrated in FIGS. **2**A and **2**B.

[0019] According to some embodiments of the present disclosure, an apparatus comprises an ESD device. The ESD device comprises a collector formed within a substrate upon which the ESD device is formed. The collector comprises a first doped region that is doped according to a first doping polarity. The ESD device comprises an emitter formed within the substrate. The emitter comprises a second doped region that is doped according to the first doping polarity. The ESD device comprises a dielectric isolation region formed between the collector and the emitter. The ESD device comprises a dielectric isolations structure. The dielectric isolation structure is formed on top of a surface of the substrate. The dielectric isolation structure is configured to provide isolation between the collector and the emitter. In an embodiment, the